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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,582	07/22/2004	Meng-Jen Wang	11182-US-PA	4581

31561 7590 03/15/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
ROMAN, ANGEL	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,582	WANG, MENG-JEN	
	Examiner	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 July 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The Declaration documents filed 07/22/04 are acceptable.

Drawings

2. The Drawings filed 07/22/04 are acceptable.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1 and 3-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Honda U.S. Patent 6,696,764 B2.

Regarding claim 1, Honda discloses a method of fabricating a flip chip ball grid array package, comprising; providing a substrate 12 comprising a first surface and a second surface, wherein the first surface comprises a plurality of cavities (see figure 8A); adhering a plurality of flip chips 13 to the cavities of the substrate 12 (see figure 9A); filling an underfill material 15 between the substrate 12 and the flip chips 13 (see figure 9B); performing a ball placement step for attaching a plurality of solder balls 16 to the second surface of the substrate (see figure 9B); and singulating the substrate 12 for separating portions of the substrate having the flip chips adhered thereon (see column 11, lines 61-65).

Regarding claim 3, Honda discloses providing the substrate 12 by providing a substrate core layer 1; forming a circuit layer 2 over the substrate core layer 1; and forming a plurality of openings in the substrate core layer 1 to exposed portions of the circuit layer 2 (see figure 8A).

Regarding claim 4, Honda discloses the circuit layer comprising a multi-layer structure comprising at least a dielectric layer 3a and a plurality of conductive layers (6, 6a) wherein the dielectric layer 3a is sandwiched between two of the conductive layers (6, 6a) (see figure 6c).

Regarding claim 5, Honda discloses forming the openings using an etching method (see column 11, lines 1-10).

Regarding claim 6, Honda teaches adhering a plurality of flip chips to the cavities by adhering each of the flip chips to each of the cavities respectively.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song U.S. Patent 6,031,284 A in view of Honda U.S. Patent 6,696,764 B2.

Regarding claim 1, Song discloses a method of fabricating a flip chip ball grid array package, comprising; providing a substrate 10 comprising a first surface and a second surface, wherein the first surface comprises a plurality of cavities (see figure 2); adhering a flip chip 20 to the cavities of the substrate 10 (see figure 3); filling an underfill material 60 between the substrate 10 and the flip chip 20 (see figure 4C); and performing a ball placement step for attaching a plurality of solder balls 80 to the second surface of the substrate 10 (see figure 4E).

Regarding claim 2, Song discloses a glue-sealing step for filling a sealing glue material 70 into the cavity to cover the flip chip 20 after the step of filling the underfill material 60 (see figure 4D).

Song is applied as above but lacks anticipation on adhering multiple flip chips in cavities form in a substrate and singulating the substrate to form individual devices. Honda discloses adhering multiple flip chips in cavities form in a substrate and singulating the substrate to form plural individual devices; in view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to form plural individual devices as disclose in Honda to form the device disclose in the primary reference of Song in order to reduce processing costs by mass-producing the devices.

8. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. U.S. Patent 6,570,469 B2 in view of Honda U.S. Patent 6,696,764 B2.

Regarding claim 1, Yamada discloses a method of fabricating a flip chip ball grid array package, comprising; providing a substrate 15 comprising a first surface and a second surface, wherein the first surface comprises a cavity (see figure 3); adhering a flip chip 4 to the cavity of the substrate 15 (see figure 3); and filling an underfill material 6 between the substrate 15 and the flip chip 4 (see figure 4).

Regarding claim 7, Yamada discloses adhering more than one flip chip in a substrate cavity (see figure 4).

Yamada et al. is applied as above but lacks anticipation on performing a ball placement step for attaching a plurality of solder balls to the second surface of the substrate 15 and adhering multiple flip chips in cavities form in a substrate and singulating the substrate to form individual packaged devices. Honda teaches a ball placement step for attaching a plurality of solder balls to the second surface of a substrate; adhering multiple flip chips in cavities form in a substrate and singulating the substrate to form individual devices; in view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to form solder balls as disclosed in Honda in the primary reference of Yamada et al. in order to provide electrical contacts for attaching the packaged device to an outside

circuit and to form plural packaged devices as disclosed in Honda in the primary reference of Yamada in order to reduce processing costs by forming plural packaged devices.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Murayama et al. and Uchida disclose method for fabricating flip chip devices in cavities.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (571) 272-1681. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER

AR
March 10, 2005